ABSTRACT OF THE DISCLOSURE

A system-on-chip integrated circuit 2 is provided with multiple data processing circuits 4, 6, 8 each with an associated diagnostic interface circuit 16, 18, 20 connected via a diagnostic transaction bus 14 to a diagnostic transaction master circuit 12. The diagnostic master transaction circuit 12 issues diagnostic transaction requests to the diagnostic interface circuits 16, 18, 20. If the associated data processing circuits 4, 6, 8 are powered-down, or otherwise non responsive, then the diagnostic interface circuit 16, 18, 20 returns a diagnostic bus transaction error signal to the diagnostic transaction master circuit 12. A sticky-bit latch 30 within each diagnostic interface circuit 16, 18, 20 serves to record a power-down event and force generation of the diagnostic bus transaction error signal until that sticky bit is cleared by the diagnostic mechanisms . This ensure the diagnostic mechanisms are made aware of the power-down event so they may take any appropriate remedial action that might be necessary as a result of that power-down event.

[Figure 4]